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# Low Power and High Speed BCD Adder using Reversible Gates

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***Abstract* — Reversible logic is one of the emerging technologies having promising applications in quantum computing. In this work, we present new design of the reversible BCD adder that has been primarily optimized for the number of ancilla input bits and the number of garbage outputs. Optimization of ancilla input bits and the garbage outputs may degrade the design in terms of the quantum cost and the delay. Firstly, we propose a new design of the reversible ripple carry adder having the input carry *C*0 and is designed with no ancilla input bits. The proposed reversible ripple carry adder design with no ancilla input bits has less quantum cost and the logic depth (delay) compared to its existing counterparts. The reversible design of the BCD adder is presented which is based on a 4 bit reversible binary adder to add the BCD number, and finally the conversion of the binary result to the BCD format using a reversible binary to BCD converter.**

***Index Terms*— ancilla inputs, garbage outputs, Quantum Cost, Reversible ripple carry adder.**

## I. INTRODUCTION

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications like advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This presents an optimized reversible BCD adder using a new reversible gate [3].

Previous addition circuits required linearly many ancillary *qubits*; our new linear depth ripple-carry quantum addition circuit uses only a single ancillary *qubit*. Also, our circuit has lower depth and fewer gates than previous ripple-carry adders [7].

The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, Toffoli gate, new gate Sayem gate and Peres gate etc. It also gives idea about basic reversible gate to build more complicated circuits which can be implemented in ALU, some sequential circuits as well as in some combinational circuits [5, 6].

Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. Adders are fundamental building blocks in many computational units. Among all the other adders, the main virtue of BCD adders is that it allows easy conversion to decimal digits for printing or display and faster decimal calculations [9].

## II. PROBLEM STATEMENT

### A. *Existing System*

In the existing system the number of *ancilla* inputs and garbage outputs are high. From this *ancilla* inputs and garbage outputs quantum cost and delay are high. Quantum cost and delay are considered as optimization parameters. To overcome this problem we design new reversible BCD adder. In 2010, carry select and carry look-ahead BCD adders using reversible logic. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. Adders are fundamental building blocks in many computational units. For this reason, we have simulated several adder circuits using the reversible gates. Among all the other adders, the main virtue of BCD adders is that it allows easy conversion to decimal digits for printing or display and faster decimal calculations.

### B. *Proposed System*

The proposed system focuses on the design of the reversible BCD adder primarily optimized for number of *ancilla* input bits and the garbage outputs. As the optimization of *ancilla* input bits and the garbage outputs may degrade the design in terms of the quantum cost and the delay, thus quantum cost and the delay parameters are also considered for optimization with primary focus towards the optimization of number of *ancilla* input bits and the garbage outputs.

## III. REVERSIBLE GATES

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A

reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- *The number of Reversible gates*: The number of reversible gates used in circuit.
- *The number of constant inputs*: This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- *The number of garbage outputs*: This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- *Quantum cost*: This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

Reversible gates used in our system are:

### *3.1 NOT gate*

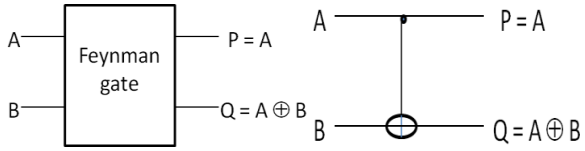
A NOT gate is a 1×1 gate represented as shown in Fig 1. Since it is a1×1 gate, its quantum cost is unity. The Figure also shows the truth table for NOT gate. If A=1 then P=0 and for A=0 then P=1.


| A | P |
|---|---|
| 1 | 0 |
| 0 | 1 |

**Fig. 1: NOT Gate**

### *3.2 CNOT gate*

The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2-input 2-output reversible gate having the mapping (A, B) to (P = A, Q = A xor B) where A, B are the inputs and P, Q are the outputs, respectively. Since it is a 2×2gate, it has a quantum cost of 1. A Fig. 2 shows the block diagrams and quantum representation of the CNOT gate.

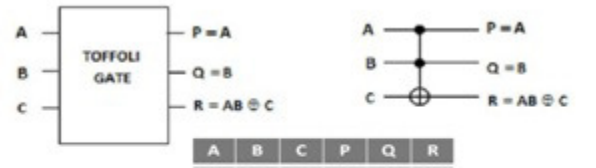



| A | B | P | Q |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

**Fig 2: CNOT Gate**

### *3.3 Toffoli gate*

A Toffoli Gate (TG)[5] is a 3x3 two through reversible gate as shown in figure 3 . Two through means two of its outputs are the same as inputs with the mapping (A, B, C) to (P =A, Q = B, R = A .B xor C), where A, B, C are inputs and P, Q, R are outputs, respectively [5].Toffoli gate is one of the most popular reversible gates and has quantum cost of 5. The quantum cost of Toffoli gate is 5.figure 3 shows the truth table for Toffoli gate. The output P and Q is same as the inputs A and respectively. The output R is AB xor C.

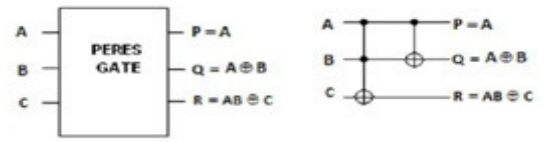



| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

**Fig. 3: TOFFOLI Gate**

### *3.4 PERES gate*

Figure 4 shows a 3x3 Peres gate [6]. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P = A, Q = A xor B and R=AB xor C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost[7]. Fig. 4 shows the truth table for Peres gate. The output P is same as the A and output Q is xor operation between A and B. The output R is (A.B) xor C).

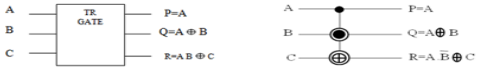



| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

**Fig. 4: PERES Gate**

*3.5 TR gate*

The reversible TR gate is an improved version of toffoli gate and it has 3 inputs , 3 outputs gate having inputs to outputs mapping as (p=A,Q=A xor B , R=(A.(notB)xor C). Fig. 5 shows the truth-table, block diagram and equivalent circuit of TR gate.




| A | B | C | P | Q | R |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

**Fig. 5: TR Gate**

## IV. Reversible Logic

High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by un-computing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as *nano* circuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required [2]. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable.

## V. Design of Reversible BCD Adder

A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit, also in BCD.

*Design of conventional BCD adder:* Instead of using the detection and the correction unit to convert the result of summation to the BCD format[7], the outputs of the binary adder can be passed to a binary to BCD converter to have the result of the binary addition in the BCD format [8][9]. This approach is illustrated in the Fig. 6.Where the 5 bit binary to BCD converter produces the desired output in the BCD format[10]. The reversible design of these two approaches used to design the reversible BCD adder to optimized for the number of *ancilla* input bits and the number of garbage outputs.

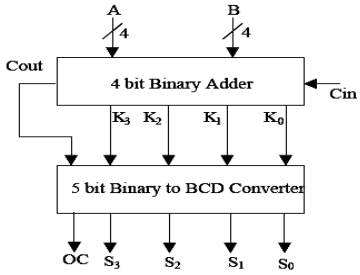



**Fig. 6: Conventional BCD adder**

**A.** *Design of Reversible BCD adder:* The proposed design of the reversible BCD adder is shown in Fig. 7 in which the input carry Cin is represented by C0, OC represents the carry out of the 4 bit reversible binary adder, and OC represents the output carry of the 1 digit BCDadder[10]. The proposed reversible BCD adder design has 1ancilla input bit and zero garbage outputs.The quantum cost of the proposed reversible BCD adder with input carry is 70 while the delay is 57.Fig. 8 shows the schematic representation of proposed design.

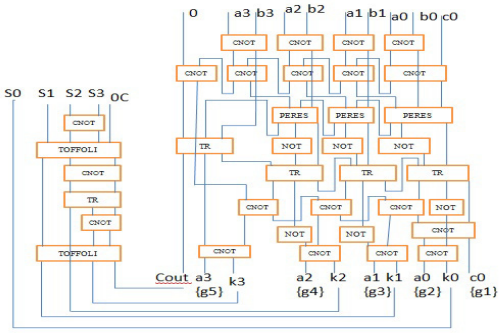



**Fig. 7: Block Diagram of proposed Design**

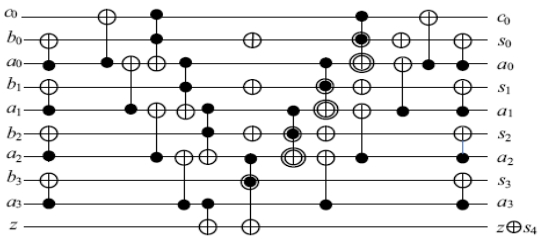



**Fig. 8: Schematic Representation of proposed design**

**B.** *Algorithm and Flow chart for reversible BCD adder:*
*Algorithm:*
STEP. 1 : Clear previous outputs.
STEP. 2 : Read inputs.
STEP. 3 : Adding inputs.
STEP. 4 : Check the conditions, if condition is satisfied add 6 to sum Otherwise store the result.
STEP. 5 : Exit.

*Flow chart:*
Fig. 8 shows the flow chart for reversible BCD adder. First reset all previous carry and inputs. Then read the inputs A, B, Cin, and add the inputs. If sum is greater than 9 or carry generated from the carry bit add 6 to the sum otherwise sum is remain as it is.

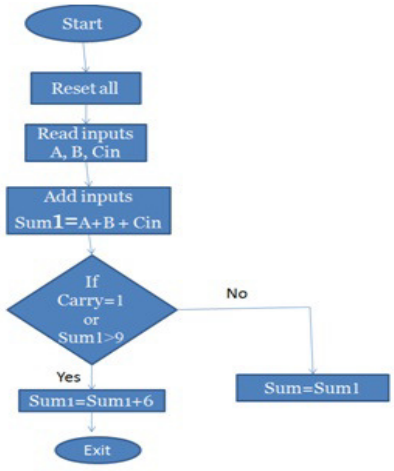



**Fig. 9: Flow chart of BCD adder**

## VI. EXPERIMENTAL RESULTS

*A. Calculation*

A, B and Cin are the inputs. S and OC are the outputs. When A= 1001, B= 1001 and Cin=0. The output is s= 1000 and output carry OC is 1.Fig. 9 shows the calculation.

**CALCULATION:**

consider the addition of two numbers

ai= 1 0 0 1
bi= 1 0 0 1
cin=0

| | |
|---|---|
| 1 0 0 1 | 9 |
| 1 0 0 1 | 9 |
| 1 0 0 1 0 | |
| 1 1 0 | |
| 1 1 0 0 0 | =18 |

co s3 s2 s1 s0

*B. Simulation Results*

The Fig. 10 simulation, we have applied the inputs a0-a3,b0-b3 and c0. a, b and c0 are the inputs. s and oc are the outputs. When A= 1001, B= 1001 and c0=0. The output is s=1000 and output carry OC is 1.Fig.11 shows the output BCD addition.


**Fig.10: Simulation with applied the inputs**

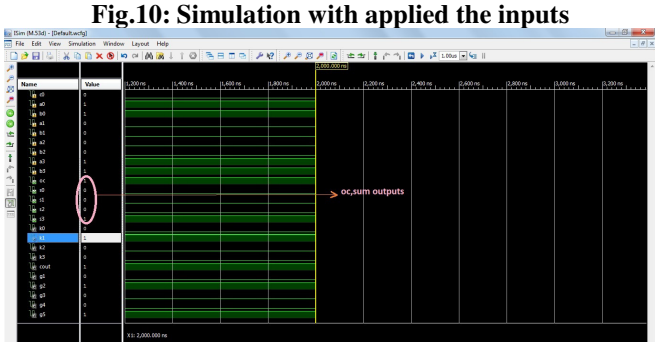



**Fig. 11: Simulation shows the sum output**

*C. RTL Schematic*

The figure 12 shows the RTL schematic of top module for reversible BCD adder, it contains inputs a, b each of which contains 4 bits and cin is the input carry. The S is the output which contains 4 bits and OC is the output carry the fig 13shows the RTL Schematic of Binary adder and Converter witha0-a3,b0-b3,co as inputs,s0-s3 and oc as outputs. The figure 14 shows the internal RTL schematic for reversible Binary to BCD converter.


**Fig. 12: RTL schematic of top module**

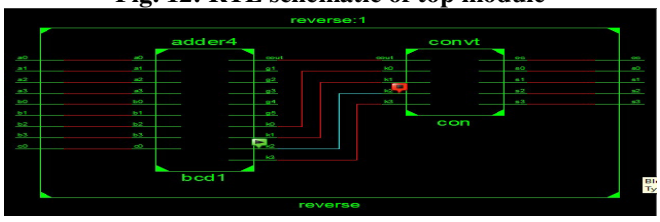



**Fig. 13: RTL schematic for Binary adder and Converter.**

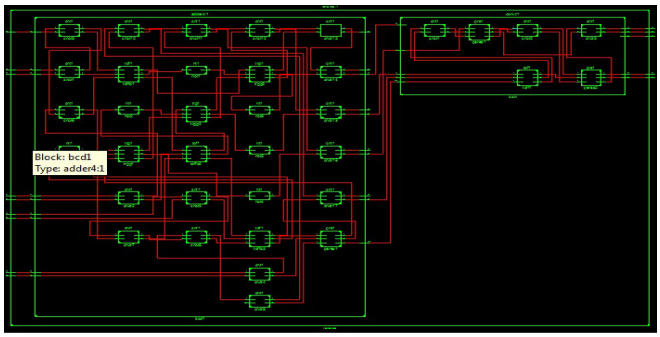



**Fig. 14: Final Schematic Generation**

## VII. CONCLUSION

In this project work, We have presented efficient designs of reversible ripple carry binary and BCD adders primarily optimizing the parameters of number of *ancilla* input bits and the garbage outputs. In the existing system the *ancilla* inputs are two and garbage outputs are twenty-one, but in our project the number of *ancilla* inputs is reduced to one and garbage outputs are reduced to zero. The optimization of the quantum cost and the delay are also considered. In the existing system quantum cost is 103 but in our project it is reduced to 70. As Compare to Conventional BCD adder the delay of the reversible BCD adder is reduced by the factor of 1.107ns. We conclude that the use of the specific reversible gates for a particular combinational function can be very much beneficial in minimizing the number of *ancilla* input bits, garbage outputs, quantum cost and the delay.

## VIII. ADVANTAGES AND APPLICATIONS

*Advantages*

a) : Low power consumption.
b) : Speed is high.
c) : Size is less compared to normal BCD adder.
d) : The reversible BCD adder can be used as a basic circuit for constructing other reversible BCD arithmetic circuits.

*Applications*

Reversible BCD adder finds its applications in Low power CMOS, Quantum computing, Nanotechnology and optical computing, Filter design, Oscillator design, Modulator and demodulator design.

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